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# UNITED STATES PATENT AND TRADEMARK OFFICE
# CERTIFICATE OF CORRECTION

PATENT NO. : 7,005,852 B2 

DATED : February 28, 2006

INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims:**

In Column 44, please add the following claims after claim 31:

--32. A liquid crystal display (LCD) device, comprising:

a display panel having a front substrate, a back substrate, a layer of liquid crystals between the front and back substrates, and an electrode layer for applying electric fields to the layer of liquid crystals, the liquid crystals and the electrode layer defining a plurality of basic visible elements;

all-metal electronics formed on the back substrate of the display panel, the all metal-electronics comprising control switches for directly controlling operation of the basic visible elements, digital-to-analog converters (DACs) for converting image data to control the control switches, frame memory for storing the image data, and selection circuitry for enabling individual ones of the basic visible elements.--

MAILING ADDRESS OF SENDER:

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--33. The LCD device of claim 32 wherein the control switches and the DACs are implemented with transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

--34. The LCD device of claim 33 wherein the frame memory comprises a plurality of blocks of all-metal memory, at least one of the blocks of memory being associated with each of the basic visible elements and being operable to store the image data therefor.--

--35. The LCD device of claim 34 wherein each basic visible element comprises a pixel having a plurality of subpixels, each subpixel corresponding to and being controlled by one of the control switches, one of the DACs, and one of the blocks of memory.--

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--36. The LCD device of claim 35 wherein each of the memory blocks is operable to store at least one bit of the image data.--

--37. The LCD device of claim 34 wherein the control switches, the DACs, and the memory blocks are arranged in a plurality of stacked levels of the all-metal electronics.--

--38. The LCD device of claim 37 wherein the control switches, the DACs, and the memory blocks associated with each basic visible element comprises one of a plurality of interchangeable circuit modules.--

--39. The LCD device of claim 32 wherein the frame memory comprises a plurality of memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--40. The LCD device of claim 39 wherein each multi-layer structure comprises:

a plurality of magnetic layers, at least one of the magnetic layers being for magnetically storing one bit of information; and

a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect;

wherein the magnetic layers are part of a substantially closed flux structure.--

--41. The LCD device of claim 32 wherein the selection circuitry comprises a plurality of transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

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PATENT NO. : 7,005,852 B2 
DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--42. The LCD device of claim 41 wherein first ones of the transpinnors are configured as drivers, and second ones of the transpinnors are configured as logic gates which are operable as selection logic.--

--43. A light-emitting diode (LED) display device, comprising:

a display panel having a substrate and a plurality of LEDs on the substrate defining a plurality of basic visible elements; and

all-metal electronics formed on the substrate of the display panel, the all metal-electronics comprising control switches for directly controlling operation of the basic visible elements, digital-to-analog converters (DACs) for converting image data to control the control switches, frame memory for storing the image data, and selection circuitry for enabling individual ones of the basic visible elements.--

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PATENT NO. : 7,005,852 B2

DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--44. The LED display device of claim 43 wherein the control switches and the DACs are implemented with transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

--45. The LED display device of claim 44 wherein the frame memory comprises a plurality of blocks of all-metal memory, at least one of the blocks of memory being associated with each of the basic visible elements and being operable to store the image data therefor.--

--46. The LED display device of claim 45 wherein each basic visible element comprises a pixel having a plurality of subpixels, each subpixel corresponding to and being controlled by one of the control switches, one of the DACs, and one of the blocks of memory.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--47. The LED display device of claim 46 wherein each of the memory blocks is operable to store at least one bit of the image data.--

--48. The LED display device of claim 45 wherein the control switches, the DACs, and the memory blocks are arranged in a plurality of stacked levels of the all-metal electronics.--

--49. The LED display device of claim 48 wherein the control switches, the DACs, and the memory blocks associated with each basic visible element comprises one of a plurality of interchangeable circuit modules.--

--50. The LED display device of claim 43 wherein the frame memory comprises a plurality of memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--51. The LED display device of claim 50 wherein each multi-layer structure comprises:

a plurality of magnetic layers, at least one of the magnetic layers being for magnetically storing one bit of information; and

a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect;

wherein the magnetic layers are part of a substantially closed flux structure.--

--52. The LED display device of claim 43 wherein the selection circuitry comprises a plurality of transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--53. The LED display device of claim 52 wherein first ones of the transpinnors are configured as drivers, and second ones of the transpinnors are configured as logic gates which are operable as selection logic.--

--54. A plasma display device, comprising:

a plasma display panel having a substrate, the display panel defining a plurality of basic visible elements;

all-metal electronics formed on the substrate of the display panel, the all metal-electronics comprising control switches for directly controlling operation of the basic visible elements, digital-to-analog converters (DACs) for converting image data to control the control switches, frame memory for storing the image data, and selection circuitry for enabling individual ones of the basic visible elements.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--55. The plasma display device of claim 54 wherein the control switches and the DACs are implemented with transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

--56. The plasma display device of claim 55 wherein the frame memory comprises a plurality of blocks of all-metal memory, at least one of the blocks of memory being associated with each of the basic visible elements and being operable to store the image data therefor.--

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DATED : February 28, 2006
INVENTOR(S) : Andrei et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--57. The plasma display device of claim 56 wherein each basic visible element comprises a pixel having a plurality of subpixels, each subpixel corresponding to and being controlled by one of the control switches, one of the DACs, and one of the blocks of memory.--

--58. The plasma display device of claim 57 wherein each of the memory blocks is operable to store at least one bit of the image data.--

--59. The plasma display device of claim 56 wherein the control switches, the DACs, and the memory blocks are arranged in a plurality of stacked levels of the all-metal electronics.--

--60. The plasma display device of claim 59 wherein the control switches, the DACs, and the memory blocks associated with each basic visible element comprises one of a plurality of interchangeable circuit modules.--

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DATED : February 28, 2006
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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--61. The plasma display device of claim 54 wherein the frame memory comprises a plurality of memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance.--

--62. The plasma display device of claim 61 wherein each multi-layer structure comprises:

a plurality of magnetic layers, at least one of the magnetic layers being for magnetically storing one bit of information; and

a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect;

wherein the magnetic layers are part of a substantially closed flux structure.--

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Claims (continued):**

--63. The plasma display device of claim 54 wherein the selection circuitry comprises a plurality of transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is substantially proportional to a power current in the network of thin-film elements.--

--64. The plasma display device of claim 63 wherein first ones of the transpinnors are configured as drivers, and second ones of the transpinnors are configured as logic gates which are operable as selection logic.--

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